Optical/Electrical Circuit Simulator Written in MATLAB

Modeling a Metal Oxide Semiconductor Transistor (MOSFET)

4th Year Project Final Report

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# Abstract

A MOSFET model was created to be part of a larger circuit simulator design to work in MATLAB by adapting SPICE documentation as a fourth year project. This was done by adapting the physical device into a circuit that models physical properties using linear and non-linear electrical devices such as resistors, diodes, current sources, and capacitors. The project used MNA techniques to create the various devices to be implemented into a compact model and solve the system using Backward Euler. The model was partially completed in that the lower LEVEL1 model was completed but the higher LEVEL2 and LEVEL3 models remain incomplete but partially working.

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# 1. Introduction

The fourth year project under the supervision of Professor Tom Smy aimed to develop an existing circuit simulator in a MATLAB environment which would aid in the analysis of optical and electrical circuits using the computer aided design technique (CAD) of modified nodal analysis (MNA). The project group consisted of Thai Nguyen, Michael Debenedictis, Saad Haq, and myself. Each member was the built a device model or improve the simulator engine, I was tasked with creating a model of a metal oxide semiconductor transistor (MOSFET) device with varying degrees of complexity. The purpose of this report is to provide an overview of the development of the model I have been working on since September 2013.

## 1.1 Background

Circuit simulators are tools necessary to evaluate designs before they are fabricated. The most famous of the early simulators is SPICE, developed by Berkeley University by Larry Nagel under the supervision of Professor Don Pederson and was released in 1972. What set SPICE apart from its predecessors was the inclusion of all models needed to simulate integrated circuits and the availability of the source code for a minimal price. Today most circuit simulators run off some form of the original SPICE code [1]. The MOSFET model that will be explored in this report is based on the SPICE simulation code and results, as well as other academic resources to aid in the development of the model.

## 1.2 Motivations and Significance

The hope for this circuit simulator is to build a larger circuit incorporating each individual model developed by the group member as well as optical devices. I personally aimed to finish a working MOSFET model that Prof Smy could use in future.

## 1.3 Objectives and Specifications

The objective of this project is to modify a skeleton circuit simulator but developing it solution engine so as to allow for more complex solutions and built models of electrical devices and microelectromechanical systems (MEMS) that function the same as those models included in a SPICE simulator. More specifically I was tasked to create a MOSFET model based on the LEVEL1 through LEVEL3 SPICE models.

# 2. Professional Considerations

All fourth year projects are group projects to simulate a real world workplace scenario where engineers work together to achieve an end. There are professional considerations each group member is expected to maintain and these are discussed in this section.

## 2.1 Health and Safety

Health and Safety is always a concern for those involved in engineering work, however there is very little risk other than ergonomic related issues when developing a device model in a MATLAB environment.

## 2.2 Engineering Professionalism

Professional Engineers Ontario defines professionalism as an engineer “demonstrating competence, impartiality and reliability” [2], further more teamwork demands that each individual respects each other as well as the group supervisor. While the project was primarily individual, in that each member worked on their own piece of the simulator, when it came time to work together as a group everyone respected each other and their work.

## 2.3 Project Management

As stated above each member worked individually to develop or modify a part of the skeleton circuit simulator given to use by Prof. Smy, this meant that there were no hard deadlines other than those set by the project coordinator for the core components: Proposal, Progress Report, Project Presentation – Oral and Poster, and the Final report. However each group member was expected to meet with Prof. Smy once a week to discuss their progress and any issues they may be having so as there would be no major delays in completing their part of the simulator. Any code developed was to be shared between the group and the supervisor via Github, “a web-based hosting service for software development projects” [3] that allowed for easy viewing and shared debugging.

# 3. Theory and Techniques

The MOSFET device was first explored in *Physical Electronics* (ELEC 3908) where we discussed the correlation between processing, structure, operation and modeling. Nonetheless for this project I needed to further research the physics of the device and how best to adapt the SPICE model to MATLAB.

## 3.1 General Approach

Enrolment in *CAD for Communication Circuit* (ELEC 4506) was required for this project. Taught by Professor Michel Nakhla it went into the basic principles of CAD tools for analysis and design of circuits and system using MNA and various solving techniques including Backward Euler which was the method used to solve my MOSFET simulations.

MNA used Kirchhoff’s circuit laws to produce equation for devices in a circuit and allows for stamp implementation into the circuit equation (3.1) shown below. All linear devices are stamped into the G and C matrixes while non-linear devices are stamped into the F(V) matrix and necessitate the implementation of Newton-Raphson iteration.

|  |  |
| --- | --- |
|  | (3. ) |

The skeleton simulator given to us included various linear device stamps such as a resistor. It was done by solving for the nodal equation from the physical device and them implementing it into the matrix via MATLAB function.

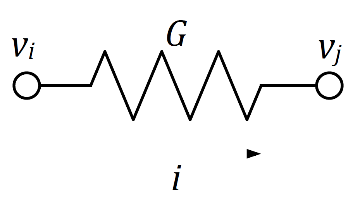


Figure : Physical Resistor Device

Nodal Equation

Figure : MNA Stamp in the G matrix

Basic MATLAB code developed in ELEC 4506, where val represents the resistor value R and G=1/R :

global G %G Matix

if (n1 ~= 0) %If the first node is not ground (1,1 position in matrix)

G(n1,n1) = G(n1,n1) + (1/val);

elseif (n2 ~= 0) %If the first node is not ground (2,2 position in matrix)

G(n2,n2) = G(n2,n2) + (1/val);

elseif (n1 ~= 0) & (n2 ~= 0) %If neither node is ground (Diagonal postions 1,2 & 2,1)

G(n1,n2) = G(n1,n2) - (1/val);

G(n2,n1) = G(n2,n1) - (1/val);

end

Non-linear devices are modelled the same way – physical, equations, and then stamp. To solve they require the inclusion of Newton-Raphson iteration to our Backward Euler method. This add a new process to the model, the Jacobian (J).

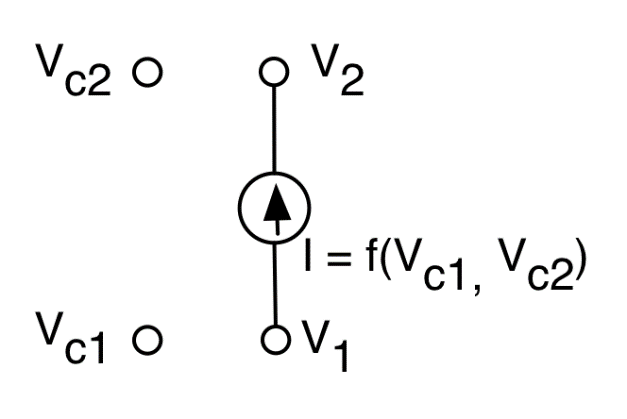


Figure : Voltage Controlled Current Source

Nodal equation

Figure : MNA stamp in the F(V) matrix

Figure : Jacobian of the system where the G matrix is empty

In this example a voltage controlled current source is modelled and its equations rely on the voltage at nodes Vc1 and Vc2 and there therefore when solving for the jacobian only those locations where the equations are derived according to those to voltages have values the others are empty. How this is implemented in the code will be explored in the following section.

Backward Euler is a first order implicit method, meaning we solve for present values using current ones over a time step “h” as shown in equation (3.2)

|  |  |
| --- | --- |
|  | (3. ) |

That when implemented with our system equation gives us equation (3.3)

|  |  |
| --- | --- |
|  | (3. ) |

Isolating for xn+1 gives us the results for the unknowns in the V matrix from equation (3.1) This method of solving the system was already in place when the group inherited the code, and thus its implementation will not be discussed in this report.

## 3.2 Specific Methods

Using the theory in the previous section as well as the original “Simulation Program with Integrated Circuit Emphasis (SPICE)” by L.W. Nagel and D.O. Pederson mentioned in the introduction and my main reference of “Semiconductor Device Modeling with SPICE” by G. Massobrio I could begin modeling the nMOS device shown in Figure 6. The term nMOS refers to a MOSFET with a p-type substrate, mean a semiconductor with a larger concentration of holes compared to electrons, a pMOS refers to the opposite, an n-type substrate with a large electron concentration. I decided to begin with an nMOS over a pMOS device due to all equations being nMOS specific and the knowledge I could allow for pMOS implementation once the nMOS was completed with a few modifications to the code. To solve for out circuit equation we must derive a circuit equivalent to the physical device shown in Figure 6, this large signal circuit is shown in Figure 7.

Figure : MOSFET Physical representation [4]

### 3.2.1 Modeling a Non-Linear Voltage Controlled Current Source Dependent on Three Voltages

With the circuit in Figure 7 we can begin modeling the channel between the source and drain represented by the current controlled voltage source IDS. The MOSFET has two primary regions of operation that I am focusing on: linear – or triode – and saturation. Where the transistor is highly depend on the voltage between the gate and the source (VGS) as it determines the concentration of carriers – holes and electrons – in the channel between the drain and the source. The voltage at which the channel just begins to connect to the source and drain is called the threshold voltage (Vth), when VGS is greater than Vth the transistor is “ON”. In what region the MOSFET is operating is depended on the voltage between the drain and the source (VDS). This is illustrated in the table below.

|  |  |  |
| --- | --- | --- |
| Region | Condition | Behaviour |
| Linear | VGS > Vth  VDS < VGS-Vth | Channel is acts as a voltage controlled resistor |
| Saturation | VGS > Vth  VDS > VGS-Vth | Channel is reduced to zero at the drain limiting the current to a constant value. |



While a threshold voltage can be assumed using experimental data the SPICE model uses equation 3.4 to calculate Vth using the flat band voltage (VFB). The flat band voltage is that between the gate and the bulk when there is an equal concentration of carriers at the surface of the gate and in the substrate, for this model the flat band voltage is assumed to be zero. The values of the surface inversion potential (2φp) and the body effect parameter (γ) where given SPICE parameters, and can be found in Appendix A. Using the values the threshold voltage for the MOSFET was found to be 0.9806 V.

Figure : Large Signal Circuit representation of an nMOS transistor [4]

|  |  |
| --- | --- |
|  | (3. ) |

To allow for better computation I created a variable BETA (β) as it is used in all SPICE LEVELs and varies only on the inputted transistor width and length, the equation is shown in equation (3.5). Again the values of the lateral diffusion (Xjl) and transconductance (KP) are constants taken from the SPICE parameters.

|  |  |
| --- | --- |
|  | (3. ) |

The value of the current passing through the channel (IDS) where calculated using the following equations in the specified regions. The channel length modulation parameter (λ) is taken from the SPICE documentation

|  |  |  |
| --- | --- | --- |
| Linear |  | (3. ) |
| Saturation |  | (3. ) |

As mentioned in Section 3.1 these equations are for a voltage controlled current source dependent on three voltages – gate, source, and drain – and thus we need to derive each according to those voltages so as to stamp them into the jacobian. Those equations are shown in the table below.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Linear |  | Saturation |  |
|  |  | (3. ) |  | (3. ) |
|  |  | (3. ) |  | (3. ) |
|  |  | (3. ) |  | (3. ) |

The implementation of these equations in a MATLAB environment are located in Appendix B.

### 3.2.2 Modeling Voltage Controlled Capacitance Dependent on Three Voltages

There are two ways of modeling the capacitances present in the MOSFET: the Meyer’s model and the Ward-Dutton model.

#### 3.2.2.1 Meyer Capacitance

The Meyer’s model for capacitance is implemented in both the LEVEL1 and LEVEL2. Three non-linear two terminal capacitors – CGB, CGS, and CGD – represent the charge-store effect present between the gate and each individual contact – bulk, source, and drain. Their location can be seen in Figure 7. Unlike the current between the drain and the source there are two extra regions of operation for these capacitors: Accumulation and Depletion. Accumulation occurs when the VGS is less than the flat band voltage, this causes holes from the substrate to accumulate on the surface. The depletion region is occurs when VGS is between VFB and Vth and a negative charge builds up in the semiconductor. The conditions for the regions are illustrated in the table below.

|  |  |
| --- | --- |
| Region | Conditions |
| Accumulation | VGS < Vth - 2φp |
| Depletion | Vth - 2φp < VGS < Vth |
| Linear | Vth­ < VGS < Vth + VDS |
| Saturation | VGS > Vth + VDS |

The equations for each capacitor are shown in the following three tables, these include the derivative that are to be stamped into the jacobian using the same method at the voltage controlled current source. The code for this model can be found in Appendix C.

Capacitance between Gate and Bulk

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Accumulation | Depletion | Saturation | Linear |
|  |  |  |  |  |
|  | 0 |  | 0 | 0 |
|  | 0 | 0 | 0 | 0 |
|  | 0 |  | 0 | 0 |

Capacitance between Gate and Drain

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Accumulation | Depletion | Saturation | Linear |
|  |  |  |  |  |
|  | 0 | 0 | 0 |  |
|  | 0 | 0 | 0 |  |
|  | 0 | 0 | 0 |  |

Capacitance between Gate and Bulk

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Accumulation | Depletion | Saturation | Linear |
|  |  |  |  |  |
|  | 0 |  | 0 |  |
|  | 0 |  | 0 |  |
|  | 0 | 0 | 0 |  |

#### 3.2.2.2 Ward-Dutton Capacitance Model

The added complexity of a LEVEL3 MOSFET allows for a more complex calculation of the capacitances in a MOSFET. The Ward-Dutto model defines four charges QG­, QS, QD, and QB these charges are connected from their voltages to ground. The model also includes the trans-capacitances, which are illustrated in Figure 8, the previously calculated Meyer capacitances are still present in these trans-capacitances. This model also allows for charge conservation which allows us to implement easier calculations for one node, in this case the source.

Figure : MOSFET Circuit representation including Ward-Dutton Capacitance

The equations for the Q capacitances in their respective regions are outlined below, the code for this model was adapted from C code given to be by Prof Smy. Therefore the equations are derived from the code and for the sake of legibility the following variables where calculated separately. The code used to model these devices can be found in Appendix D.

|  |  |
| --- | --- |
|  | (3. ) |
|  | (3. ) |
|  | (3. ) |
|  | (3. ) |
|  | (3. ) |
|  |  |

|  |  |
| --- | --- |
|  | Accumulation |
|  |  |
|  |  |
|  | 0 |
| cggb |  |
| cgdb | 0 |
| cgbb | 0 |
| cgsb |  |
| cbgb | 0 |
| cbdb | 0 |
| cbbb | 0 |
| cbsb | 0 |
| cdgb | 0 |
| cddb | 0 |
| cdbb | 0 |
| cdsb | 0 |

|  |  |
| --- | --- |
|  | Depletion |
|  |  |
|  |  |
|  | 0 |
| cggb |  |
| cgdb | 0 |
| cgbb | 0 |
| cgsb |  |
| cbgb | 0 |
| cbdb | 0 |
| cbbb | 0 |
| cbsb | 0 |
| cdgb | 0 |
| cddb | 0 |
| cdbb | 0 |
| cdsb | 0 |

|  |  |  |
| --- | --- | --- |
|  | Linear | |
|  |  | |
|  |  | |
|  |  | |
| cggb |  | |
| cgdb |  | |
| cgbb |  | |
| cgsb |  | |
| cbgb |  | |
| cbdb |  | |
| cbbb |  | |
| cbsb |  | |
| cdgb |  | |
| cddb |  | |
| cdbb |  | |
| cdsb |  | |
|  | Saturation |
|  |  |
|  |  |
|  |  |
| cggb |  |
| cgdb | 0 |
| cgbb |  |
| cgsb |  |
| cbgb |  |
| cbdb | 0 |
| cbbb |  |
| cbsb |  |
| cdgb |  |
| cddb | 0 |
| cdbb |  |
| cdsb |  |

|  |  |
| --- | --- |
|  | In Every Region |
| Qs |  |
| CSGB |  |
| CSDB |  |
| CSSB |  |
| CSBB |  |

# 4. Achievements

While there were various difficulties, being it buggy code, convergence issues, or interfering coursework I was able to get a full LEVEL1 MOSFET model working and a partial LEVEL3 with Ward-Dutton capacitances.

## 4.1 Results

This section will break down the results of the individual pieces that make up the MOSFET model.

### 4.1.1 Voltage Controlled Current Source Dependent on Three Voltages

The following figure is the result of the current passing through the channel from drain to source with the following parameters. Note – Start Voltage: Increment: End Voltage

|  |  |
| --- | --- |
|  | Value |
| VG | 2:1:5 V |
| VD | 0:1:5 V |
| VS | 0 V |
| VB | 0 V |
| W | 100 µm |
| L | 100 µm |

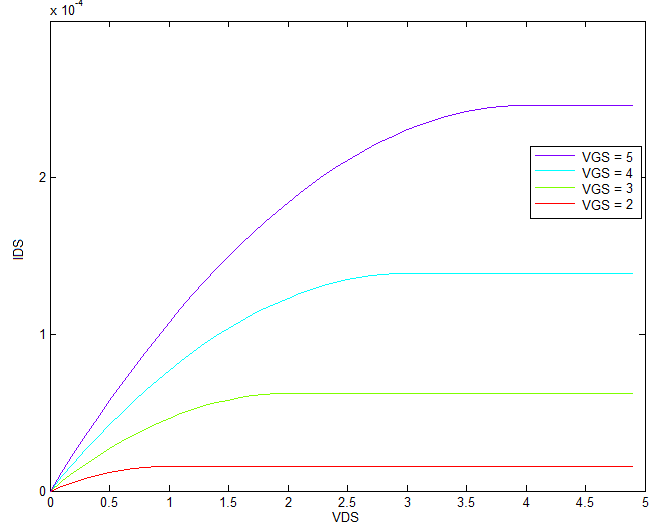


Figure : Results of IDS versus VDS – MATLAB

When compared to the results taken from the SPICE simulation in Figure 10 with the same parameters the model voltage controlled current source modeling the IDS current is near exact. This may be caused by the diode model used to model those in Figure 6 in section 3, that model uses the ideal diode equation instead of the exact equations used by the SPICE software. The values were deemed successful enough to move onto the Meyer’s capacitance models.

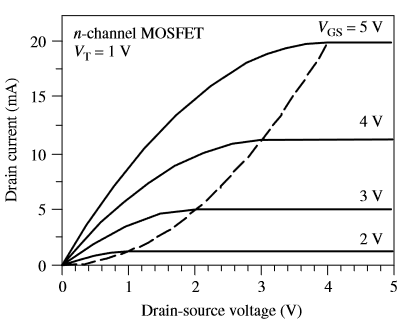


Figure : SPICE simulation of IDS versus VDS

### 4.1.2 Meyer’s Gate Capacitances

The Meyer’s gate capacitance simulations where successful as well as shown by the direct comparison of figure 11 and 12. While the CGB capacitance in figure 12 does not drop off suddenly as shown in figure 11 this is caused by the limited time steps taken by the simulation, due to the intricacy of the code running the transient simulation I was unable to fix this issue.

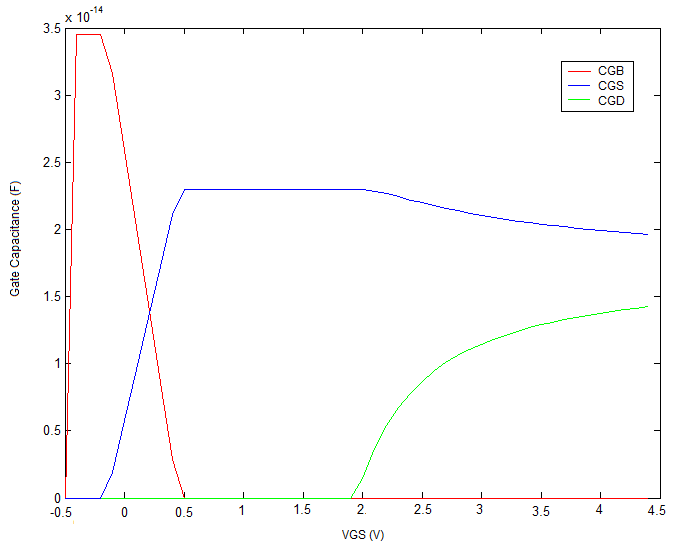
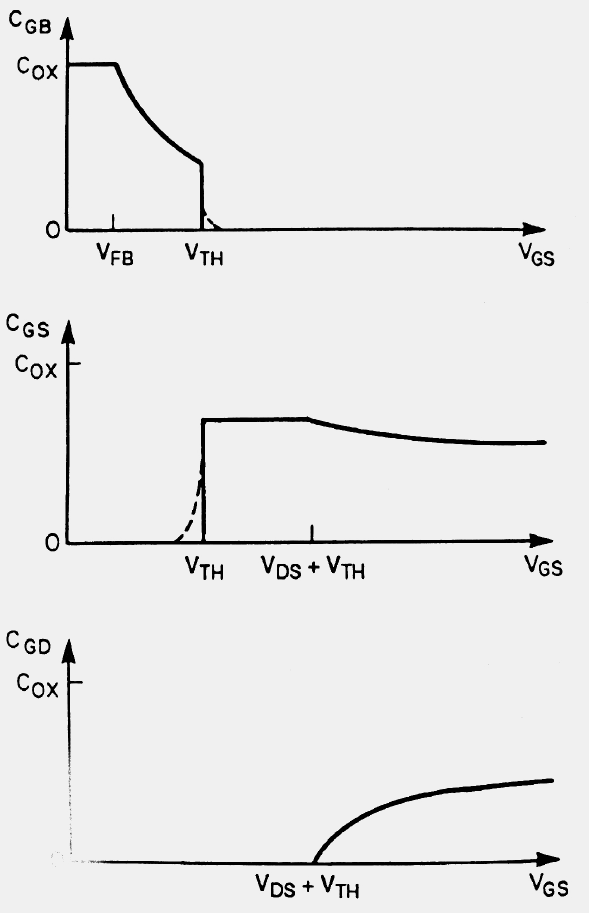


Figure : SPICE Results of Meyer's Model Gate Capacitances

Figure : Gate Capacitance over a ramping VGS

### 4.1.3 Ward-Dutton Capacitances

The best way of illustrating the precision of the Ward-Dutton over the Meyer is to compare the IDS current and the voltages seen at the gate and the drain with a 0 to 2 volt pulse at the gate. As the voltage increases the MOSFET turns on and drives the drain voltage down. The Ward-Dutton more accurately models how the physical device reacts in this scenario, the transitions are smoother and the values more accurate.



Figure : Nodal Voltages reacting to Voltage Pulse with either Meyer or Ward-Dutton Capacitances

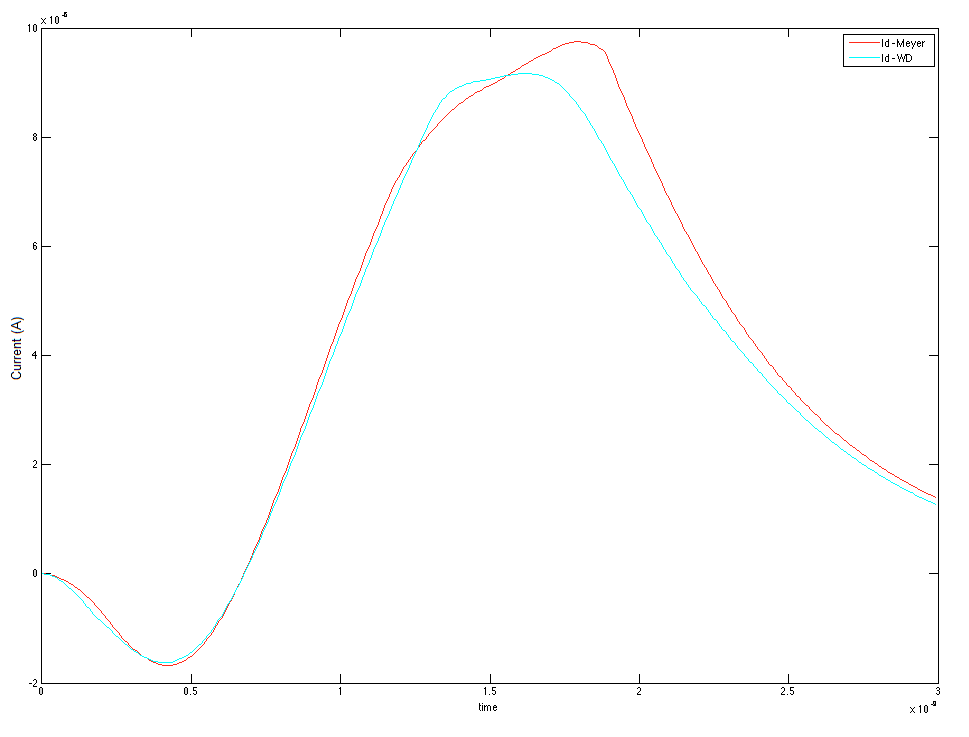


Figure : Drain-Source Current reacting to a Voltage pulse with either Meyer or Ward-Dutton Capacitances

# 5. Conclusion

The aim of the project was to create a working simulator that had a working MOSFET model, I feel that the results I have gotten from my code represents a partially working MOSFET model. There is still much that needs to be completed and will be discussed in the following section. However I do believe I have learned a great deal about the modeling of devices and the amount of physics, mathematics, code and time that goes into creating a tool like Cadence or ADS that run off SPICE models. As a group we presented our modified simulator too two faculty members in a twelve minute presentation and then presented the material to the University via the poster presentations. I believe that both presentations went well and I believed a contributed an equal part to the overall group of this project.

## 5.2 Contributions

I have built a working LEVEL1 MOSFET model that allows for some parameter customization, this model consists of two linear resistors and six non-linear devices: two diodes, three voltage controlled capacitors and one voltage controlled current source. I have a somewhat working LEVEL3 model that is able to model Ward-Dutton capacitances that produces accurate comparison to the working Meyer’s capacitances.

## 5.3 Future Work

If I had more time I would have liked to:

* Fully complete the LEVEL3 MOSFET by implementing the more complex IDS current equations
* Allow for pMOS creation
* Try again at implementing the full LEVEL2 model that includes short channel effects.

# References

|  |  |
| --- | --- |
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| [3] | Wikipedia, "GitHub," 1 April 2014. [Online]. Available: http://en.wikipedia.org/wiki/GitHub. |
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# Appendix A

The following table consists of the constant parameters used in the simulations that produced the figures in section 4.2.

|  |  |  |
| --- | --- | --- |
| Name |  | Value |
| lamda | Channel Length Modulation | 0.02 |
| twophip | Surface inversion potential | 0.58 |
| gama | Body-effect parameter | 0.526 |
| eps | For Silicon | (8.85e-14)(11.8) |
| DELTA | Width effect on threshold voltage | 1 |
| Cox | Capacitance per unit area of thin oxide | (3.45e-13)/(1e-7) |
| KP | Transconductance parameter | 3e-5 |
| Xjl | Lateral diffusion | 0.8e-6 |
| Xj | Metallugical junction depth | 10e-6 |
| phij | Bulk junction potential | 0.75 |
| Na | Substrate doping | 10e15 |
| q | Charge on an electron | 1.60e-19 |
| Xd | Coefficient of the depletion Region | sqrt((2eps)/(q\*Na)) |
| rS | Source Resistance | 10 |
| rD | Drain Resistance | 10 |
| Nss | Surface State Density | 10e10 |
| tox | Thin Oxide Thickness | 10e-7 |
| eox | Permittivity of the Oxide | (8.85e-14)(3.9) |
| VFB | Flat Band Voltage | 0 |
| delta |  | 0.5 |
| VT | Threshold Voltage | VFB+twophip+gma\*sqrt(twophip) |

# Appendix B

The pages that follow are the code for the MOSFET, it primarily deals with the voltage controlled current source IDS while implementing the other components of the large signal circuit in Figure 7 via imported models developed by Michael Debenedictis, Prof. Tom Smy, and myself.

# Appendix C

Meyer’s Capacitance Model Code

# Appendix D

Ward-Dutton Capacitance Code